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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	K. SUZUKI, et al.
Application No.:	Rule 1.53(b) Divisional of U.S. Patent Application Serial No. 09/959,576, filed October 30, 2001
Filed:	On even date herewith
For:	METHOD OF MANUFACTURING A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE HAVING A PLURALITY OF WIRING LAYERS AND MASK-PATTERN GENERATION METHOD (As Amended)
Art Group of Parent:	2811
Examiner of Parent:	S. Hu

PRELIMINARY AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

October 21, 2003

Sir:

Prior to examination, please amend the above-identified application as listed below and as set forth on the following pages:

Amendments to the Specification and Title

Remarks are included following the amendments.